uP7534

Current-Limited, Power Distribution Switches

General Description

The uP7534 is a current limited high-side switch designed for applications where heavy capacitive loads and short-circuits are likely to be met. This device operates with inputs from 2.7V to 5.5V for both 3V and 5V systems. Its low quiescent current (25uA) and standby current (<1uA) conserve battery power in portable.

The power switch is controlled by a logic enable input and driven by an internal charge pump circuit. When the output load exceeds the current-limit threshold or a short is present, the uP7534 asserts overcurrent protection and limits the output current to a safe level by driving the power switch into saturation mode.

The uP7534 features glitch-blank fault flag that is asserted by overcurrent, overtemperature, or input undervoltage lockout. The 8ms glitch-blanking time allows momentary faults to be ignored, thus preventing false alarms to the host system.

Other features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present. The uP7534 is available in SOP-8, SOT23-5, MSOP-8, and PMSOP-8 packages.

Features

- Compliant to USB Specifications
- Operating Range: 2.7 V to 5.5 V
- 75mΩ (5VIN MSOP) High Side MOSFET Switch
- 25uA Typical Quiescent Current
- <1uA Typical Shutdown Current
- Over Current/ Short Circuit Protect
- Thermal Shutdown Protection
- Deglitched Open Drain Fault Flag
- Slow Turn On and Fast Turn Off
- Enable Active-High or Active-Low
- UL Approved-E316940
- TuV EN60950-1 Certification
- CB IEC60950-1 Certification
- RoHS Compliant and Halogen Free

Applications

- Notebook and Desktop PCs
- USB Power Management
- ACPI Power Distribution
- Hot-Plug Power Supplies
- Battery-Powered Equipments
- Battery-Charger Circuits

Pin Configuration
### Ordering Information

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package</th>
<th>Top Marking</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>uP7534AS8-XX</td>
<td>SOP-8L</td>
<td>S14-A-XX</td>
<td>Enable Active High</td>
</tr>
<tr>
<td>uP7534BS8-XX</td>
<td>SOP-8L</td>
<td>S14-B-XX</td>
<td>Enable Active Low</td>
</tr>
<tr>
<td>uP7534CSA8-XX</td>
<td>SOP-8L</td>
<td>uP7534CS8-XX</td>
<td>Enable Active High</td>
</tr>
<tr>
<td>uP7534DSA8-XX</td>
<td>SOP-8L</td>
<td>uP7534DS8-XX</td>
<td>Enable Active Low</td>
</tr>
<tr>
<td>uP7534AM5-XX</td>
<td>SOT23-5L</td>
<td>S14-A-XX</td>
<td>Enable Active High</td>
</tr>
<tr>
<td>uP7534BM5-XX</td>
<td>SOT23-5L</td>
<td>S14-B-XX</td>
<td>Without Enable Pin</td>
</tr>
<tr>
<td>uP7534CMA5-XX</td>
<td>SOT23-5L</td>
<td>S14-C-XX</td>
<td>Enable Active High</td>
</tr>
<tr>
<td>uP7534DMA5-XX</td>
<td>SOT23-5L</td>
<td>S14-D-XX</td>
<td>Enable Active Low</td>
</tr>
<tr>
<td>uP7534ARA8-XX</td>
<td>MSOP-8L</td>
<td>7534AXX</td>
<td>Enable Active High</td>
</tr>
<tr>
<td>uP7534BRA8-XX</td>
<td>MSOP-8L</td>
<td>7534BXX</td>
<td>Enable Active Low</td>
</tr>
<tr>
<td>uP7534ARU8-XX</td>
<td>PMSOP-8L</td>
<td>7534AXX</td>
<td>Enable Active High</td>
</tr>
<tr>
<td>uP7534BRU8-XX</td>
<td>PMSOP-8L</td>
<td>7534BXX</td>
<td>Enable Active Low</td>
</tr>
<tr>
<td>uP7534EMA5-XX</td>
<td>SOT23-5L</td>
<td>S14-E-XX</td>
<td>Enable Active High</td>
</tr>
<tr>
<td>uP7534FMA5-XX</td>
<td>SOT23-5L</td>
<td>S14-F-XX</td>
<td>Enable Active Low</td>
</tr>
<tr>
<td>uP7534GMA5-XX</td>
<td>SOT23-5L</td>
<td>S14-G-XX</td>
<td>Enable Active High</td>
</tr>
<tr>
<td>uP7534HMA5-XX</td>
<td>SOT23-5L</td>
<td>S14-H-XX</td>
<td>Enable Active Low</td>
</tr>
</tbody>
</table>

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

### Typical Application Circuit

![Typical Application Circuit Diagram]
## Functional Pin Description

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>OC#</td>
<td><strong>Fault Flag.</strong> This is an active-low, open-drain fault flag output for the power switch. The uP7534 asserts this pin low when fault occurs with typical 8ms deglitching time delay.</td>
</tr>
<tr>
<td>VOUT</td>
<td><strong>Output Voltage.</strong> These pins are output from N-Channel MOSFET Source. Bypass this pin with a minimum 10μF capacitor to ground.</td>
</tr>
<tr>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>EN/EN#</td>
<td><strong>Enable Input.</strong> This is the enable input to turn on/off the power switch. Active high for uP7534A/C/E/G and active low for uP7534B/D/F/H</td>
</tr>
<tr>
<td>VIN</td>
<td><strong>Supply Input.</strong> This is the input pin to N-Channel MOSFET Drain and supply to control circuit. Bypass this pin with a 22μF capacitor to ground.</td>
</tr>
<tr>
<td>NC</td>
<td>Not Internally Connected.</td>
</tr>
</tbody>
</table>

## Functional Block Diagram

![Functional Block Diagram](image-url)
Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from VOUT to VIN and VIN to VOUT when disabled. The power switch is controlled by a logic enable input (active high for uP7534A/C/E/G and active low for uP7534B/D/F/H) and driven by an internal charge pump circuit. When the output load exceeds the current-limit threshold or a short is present, the uP7534 asserts overcurrent protection and limits the output current to a safe level by driving the power switch into saturation mode.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Chip Enable (for uP7534A/C/E/G)

The EN pin receives a TTL or CMOS compatible input to enable/disable the uP7534A/C/E/G Logic low disables the power switch, charge pump, gate driver and other circuitry and reduces the supply current down to less than 1uA. Logic high restores bias to the drive and control circuits and turns the switch on.

Chip Enable (for uP7534B/D/F/H)

The EN# pin receives a TTL or CMOS compatible input to enable/disable the uP7534B/D/F/H. Logic high disables the power switch, charge pump, gate driver and other circuitry and reduces the supply current down to less than 1uA. Logic low restores bias to the drive and control circuits and turns the switch on.

Soft Start

The uP7534 features soft start function to eliminate the inrush current into downstream and voltage droop of upstream when hot-plug-in with capacitive loads. The soft start interval is 0.9ms typically. The input current to charge up the load capacitor is proportional to its capacitance. The uP7534 current limit function may be active during the plug-in of extreme large capacitive load. The fault flag is masked during the softstart interval.

Over Current Limit

The uP7534 continuous monitors the output current for overcurrent protection to protect the system power, the power switch, and the load from damage during output short circuit or soft start interval. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load. The current limit level is typical 1A when the power switch operates in linear region and is typical 0.6A in saturation region (for uP7534A/BS8-06).

The uP7534 asserts fault condition and pulls low OC# when overcurrent, overtemperature, input under voltage lockout condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 8ms deglitch circuit prevents the OC# signal from oscillation or false triggering. If an overtemperature shutdown occurs, the OC# is asserted instantaneously.

Overtemperature Protection

The uP7534 continuously monitor the operating temperature of the power switch for overtemperature protection. The uP7534 asserts overtemperature and turns off the power switch to prevent the device from damage if the junction temperature rises to approximately 135°C due overcurrent or short-circuit conditions. Hysteresis is built into the thermal sense, the switch will not turns back on until the device has cooled approximately 20 degrees. The open-drain false reporting output (OC#) is asserted (active low) when an overtemperature shutdown or overcurrent occurs. If the fault condition is not removed, the switch will pulse on and off as the temperature cycles between these limits.

Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2.2V, a control signal turns off the power switch.

Output Voltage Discharge When Disabled

The output voltage is discharged through an internal 100Ω resistor when the output voltage is disabled.
Absolute Maximum Rating

Supply Input Voltage, VIN

DC

-0.3V to +6V

< 200μs, non-repetitive

-0.3V to +10V

Other Pins

-0.3V to +6V

Storage Temperature Range

-65°C to +150°C

Junction Temperature

150°C

Lead Temperature (Soldering, 10 sec)

260°C

ESD Rating (Note 2)

HBM (Human Body Mode)

2kV

MM (Machine Mode)

200V

Package Thermal Resistance (Note 3)

SOP-8 θJA

160°C/W

SOP-8 θJC

39°C/W

SOT23-5 θJA

250°C/W

SOT23-5 θJC

50°C/W

MSOP-8 θJA

160°C/W

MSOP-8 θJC

40°C/W

PMSOP-8 θJA

86°C/W

PMSOP-8 θJC

30°C/W

Power Dissipation, PD @ TA = 25°C

SOP-8

0.625W

SOP23-5

0.4W

MSOP-8

0.625W

PMSOP-8

1.16W

Recommended Operation Conditions

Operating Junction Temperature Range

-40°C to +125°C

Operating Ambient Temperature Range

-40°C to +85°C

Supply Input Voltage, V_in

+2.7V to +5.5V

Electrical Characteristics

(V_in = 5V, TA = 25°C, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Supply Input Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Under Voltage Lockout</td>
<td>V_UVLO</td>
<td>V_in rising</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>UVLO Hysteresis</td>
<td>ΔV_UVLO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>I_SD</td>
<td>No load on VOUT, Disabled</td>
<td></td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>I_Q</td>
<td>No load on VOUT, Enabled</td>
<td></td>
<td></td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>
### Electrical Characteristics

#### Chip Enable

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic High Threshold</td>
<td>$V_H$</td>
<td>$2.7V &lt; V_H &lt; 5.5V$</td>
<td>1.4</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Logic Low Threshold</td>
<td>$V_L$</td>
<td>$2.7V &lt; V_L &lt; 5.5V$</td>
<td>--</td>
<td>0.4</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Enable Input Current</td>
<td>$I_{ENP}$</td>
<td>$0V &lt; V_{ENP} &lt; 5.5V$</td>
<td>-0.5</td>
<td>--</td>
<td>0.5</td>
<td>µA</td>
</tr>
<tr>
<td>Turn On Time (Note 5)</td>
<td>$T_{ON}$</td>
<td>$C_L = 1uF$, $R_L = 10\Omega$</td>
<td>--</td>
<td>1</td>
<td>--</td>
<td>ms</td>
</tr>
<tr>
<td>Turn Off Time (Note 5)</td>
<td>$T_{OFF}$</td>
<td>$C_L = 1uF$, $R_L = 10\Omega$</td>
<td>--</td>
<td>0.3</td>
<td>--</td>
<td>ms</td>
</tr>
<tr>
<td>Output Rise Time</td>
<td>$T_{R}$</td>
<td>$C_L = 1uF$, $R_L = 10\Omega$</td>
<td>0.6</td>
<td>0.9</td>
<td>1.2</td>
<td>ms</td>
</tr>
<tr>
<td>Output Fall Time</td>
<td>$T_{F}$</td>
<td>$C_L = 1uF$, $R_L = 10\Omega$</td>
<td>--</td>
<td>0.2</td>
<td>0.5</td>
<td>ms</td>
</tr>
<tr>
<td>Output Discharge Resistance when Disabled</td>
<td></td>
<td></td>
<td>--</td>
<td>100</td>
<td>--</td>
<td>Ω</td>
</tr>
</tbody>
</table>

#### Power Switch

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-MOSFET ON Resistance</td>
<td>$R_{DS(ON)}$</td>
<td>uP7534ARA8-20, uP7534BRA8-20, $V_{IN} = 5.0V$ , $I_{OUT} = 0.5A$</td>
<td>--</td>
<td>70</td>
<td>75</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>uP7534A/B/C/D (Others), $V_{IN} = 5.0V$ , $I_{OUT} = 0.5A$</td>
<td>--</td>
<td>90</td>
<td>100</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>uP7534E/F/G/H, $V_{IN} = 5.0V$ , $I_{OUT} = 0.5A$</td>
<td>--</td>
<td>100</td>
<td>110</td>
<td>mΩ</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>$I_{OUT}$</td>
<td>VOUT connected to GND, Disabled</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>Reverse Leakage Current</td>
<td>$V_{OUT}$</td>
<td>$V_{OUT} = 5.5V$, $V_{IN} = 0V$</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>µA</td>
</tr>
</tbody>
</table>

#### Current Limit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short Circuit Output Current</td>
<td>$I_{SC}$</td>
<td>$V_{IN} = 5.0V$, VOUT connected to GND, device enabled into short-circuit</td>
<td>uP7534XXXX-06</td>
<td>--</td>
<td>0.6</td>
<td>0.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>uP7534XXXX-10</td>
<td>--</td>
<td>1.0</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>uP7534XXXX-15</td>
<td>--</td>
<td>1.5</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>uP7534XXXX-20</td>
<td>--</td>
<td>2.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Overcurrent Trip Threshold</td>
<td>$I_{SC,TRIP}$</td>
<td>$V_{IN} = 5.0V$, current ramp &lt; 100A/s on VOUT</td>
<td>uP7534XXXX-06</td>
<td>0.6</td>
<td>1.0</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>uP7534XXXX-10</td>
<td>1.1</td>
<td>1.8</td>
<td>1.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>uP7534XXXX-15</td>
<td>2.0</td>
<td>2.5</td>
<td>3.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>uP7534XXXX-20</td>
<td>2.8</td>
<td>3.3</td>
<td>5.0</td>
</tr>
</tbody>
</table>

#### Fault Flag (OC#)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Low Voltage</td>
<td>$V_{OL}$</td>
<td>$I_{OC#} = 5mA$</td>
<td>--</td>
<td>--</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Off State Current</td>
<td>$V_{OC#}$</td>
<td>$V_{OC#} = 5.5V$</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>OC# Deglitch</td>
<td></td>
<td>OC# assertion delay</td>
<td>5</td>
<td>8</td>
<td>15</td>
<td>ms</td>
</tr>
</tbody>
</table>

#### Over Current Protection

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shutdown-Level Threshold</td>
<td></td>
<td>By Design</td>
<td>--</td>
<td>135</td>
<td>--</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td></td>
<td>By Design</td>
<td>--</td>
<td>20</td>
<td>--</td>
<td>°C</td>
</tr>
</tbody>
</table>
Note 1. Stresses beyond those listed as the above Absolute Maximum Ratings may cause permanent damage to the device. These are for stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operation Condition section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. $\theta_{ja}$ is measured in the natural convection at $T_a = 25^\circ$C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. These items are not tested in production, specified by design.
Typical Operation Characteristics

- **On Resistance vs. Input Voltage**
  - Input Voltage $V_{IN} (V)$
  - On Resistance (mΩ)

- **OC# Delay Time vs. Input Voltage**
  - Input Voltage $V_{IN} (V)$
  - OC# Delay Time (ms)

- **EN/EN# Threshold Level vs. Input Voltage**
  - Input Voltage $V_{IN} (V)$
  - High/Low Threshold Level (V)
  - Low Level
  - High Level

- **Quiescent Current vs. Input Voltage**
  - Input Voltage $V_{IN} (V)$
  - Quiescent Current (μA)

- **Short Circuit vs. Input Voltage**
  - Input Voltage $V_{IN} (V)$
  - Output Short Circuit Current (A)

- **On Resistance vs. Temperature**
  - Junction Temperature (°C)
  - On Resistance (mΩ)

- **On Resistance vs. Input Voltage (SOP-8 Package)**
  - Input Voltage $V_{IN} (V)$
  - On Resistance (mΩ)
Typical Operation Characteristics

Quiescent Current vs. Temperature

EN/EN# Threshold Level vs. Temperature

Turn On Waveforms

Turn Off Waveforms

Power Off Waveforms

EN = 5V, COUT = 1uF, RLOAD = 10Ω

VOUT (2V/Div)

ILOAD (250mA/Div)

VOUT (2V/Div)

ILOAD (250mA/Div)

VOUT (2V/Div)

ILOAD (250mA/Div)

VOUT (2V/Div)
Typical Operation Characteristics

Power On Waveforms

Time (2.5ms/Div)

\( V_{IN} = 5V, \ C_{OUT} = 1uF, \ R_{LOAD} = 10\Omega \)

Short Circuit Protection and OTP

Time (4ms/Div)

\( V_{IN} = 5V, \ C_{OUT} = 470uF, \ R_{LOAD} = 0\Omega \)
Supply Input Filtering

VIN pins supply power to the power switch and internal circuit. Both of them should be connect to upstream power supply with short and wide trace on the PCB.

Events such as hot-plug/unplug, output short circuit and overtemperature result in step change of input current with sharp edges, which in turn causes voltage transient at supply input due to di/dt effect of parasitic inductance on the current path. A 0.1uF ceramic capacitor from VIN to GND, physically located near the device is strongly recommended to control the supply input transient. Minimizing the parasitic inductance along the current path also alleviate the voltage transient at the supply input.

Output Voltage Filtering

Bypassing the output voltage with a 0.1uF ceramic capacitor improves the immunity of the device against output short circuit and hot plug/unplug of load. A lower ESR capacitor results in lower voltage drop against a step load change. A large electrolytic capacitor from VOUT to GND is also recommended. This capacitor reduces power supply transient that may cause ringing on the input.

USB supports dynamic attachment (hot plug-in) of peripherals. A current surge is caused by the input capacitance of downstream device. Ferrite beads are recommended in series with all power and ground connector pins. Ferrite beads reduce EMI and limit the inrush current during hot-attachment by filtering high-frequency signals. The DC resistance of the ferrite bead should be specially taken care to reduce the voltage drop.

Voltage Drop and Power Dissipation

Temperature effect should be well considered when dealing with voltage drop and power dissipation. The maximum \( R_{DS(ON)} \) of the power switch is 100m\( \Omega \) under 25°C junction temperature. If the device is expected to operate at 125°C junction temperature, the \( R_{DS(ON)} \) will become

\[
100\text{m} \Omega \times \left(1 + (125°C - 25°C) \times 0.5%/°C \right) = 150\text{m} \Omega
\]

where 0.5%/°C is the approximated temperature coefficient of the \( R_{DS(ON)} \).

If the maximum load current is expected to be 1.2A, the maximum voltage will become

\[
1.2\text{A} \times 150\text{m} \Omega = 180\text{mV}
\]

This in turn will cause power dissipation as

\[
1.2\text{A} \times 180\text{mV} = 215\text{mW}
\]

The temperature raise is calculated as

\[
215\text{mW} \times 160 \text{°C}/\text{W} = 35°C
\]

Layout Consideration

The power circuitry of USB printed circuit boards requires a customized layout to maximize thermal dissipation and to minimized voltage drop and EMI.

- Place the device physically as close to the USB port as possible. Keep all traces wide, short and direct to minimized the parasitic inductance. This optimizes the switch response time to output short circuit conditions.
- Place both input and output bypass capacitors near to the device.
- If ferrite beads are used, use wires with minimum resistance and large solder pads to minimize connection resistance.
- All VOUT pins should be connected together on the PCB. All VIN pins should be connected together on the PCB.
Note

1. Package Outline Unit Description:
   - BSC: Basic. Represents theoretical exact dimension or dimension target
   - MIN: Minimum dimension specified.
   - MAX: Maximum dimension specified.
   - REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   - TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.
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